REMARKS

The following remarks are fully and completely responsive to the Office Action dated March 11, 2004. Claims 1, 10, 11, 18, 21-23, 26, 32 and 35-37 are pending in this application. In the outstanding Office Action, claims 32 and 37 were rejected under 35 U.S.C. §103(a). Claims 21-23 were acknowledged as containing allowable subject matter, but were objected to as being dependent on rejected base claim. No new matter has been added. Claims 21-23, 32 and 37 are presented for reconsideration.

35 U.S.C. §103(a)

Claims 32 and 37 were rejected under 35 U.S.C. §103(a) as being unpatentable over Taya (U.S. Patent No. 5,778,214). In making this rejection, the Office Action asserts that these claims are taught and/or suggested by Taya. Applicants respectfully request reconsideration of the rejection of claims 32 and 37.

Fig.12 of Taya discloses "delay elements" 11a-11n and "switches" 12a -12n. In the structure disclosed in the Fig.12 of Taya, "a signal input terminal is connected to the first of the serially-connected delay elements 11a -11n, and output sides of the delay elements 11a-11n are connected to the switches 12a -12n, respectively" (column 9, lines 32 - 36). Further, "one of outputs from the delay elements 11a -11n is provided to the buffer 15 through the corresponding switch" (column 9, lines 37 - 39). Therefore, the signal is propagated in the direction from the delay elements 11a -11n to the switches 12a -12n.

Taya further discloses, "the delay elements 11a - 11n are in the form of CMOS inverters, respectively" (column 9, lines 41 - 42). The Office Action asserted that it

would have been obvious to implement the CMOS inverters that had the same size transistors so as to let the rise time and fall time of the output signal from the inverter be substantially uniform.

Claims 32 and 37 relate to the seventh embodiment of this application, an example of which is shown in Fig. 7. In the invention of claims 32 and 37, each of the "predetermined delay stages" is "connected in series" and has an "individual input terminal". "Selecting switch means" receives an "input signal" and connects the signal to "one of the individual input terminals" of the "predetermined delay stage". And an "output signal" is output "from the delay path". Therefore, the signal is propagated in the direction from the "selecting switch means" to the "predetermined delay stage". In this structure, "each predetermined delay stage" has "substantially uniform rise delay time and fall delay time".

In the invention of claims 32 and 37, it is impossible to form the "predetermined delay stage" from primitive CMOS inverters because each of the "predetermined delay stage" has an "individual input terminal" in addition to the "serial input terminal".

Taya only discloses the implementation of CMOS inverter to the structure in which the signal is propagated in the direction from the delay elements to the switches. Thus, Taya fails to teach and/or suggest that each "predetermined delay stage" has "substantially uniform rise delay time and fall delay time" in the structure in which the signal is propagated in the direction from the "selecting switch means" to the "predetermined delay stage" that has an "individual input terminal" in addition to the "serial input terminal". Accordingly, Applicants request reconsideration and withdrawal of the rejection of claims 32 and 37 under 35 U.S.C §103(a).

Claim Objections

Claims 21-23 were objected to as being dependent upon rejected base claim. Claims 21-23 are dependent upon claim 32, which is allowable for the reasons discussed above. Therefore Applicants request the withdrawal of the objection to claims 21-23.

Conclusion

Applicant's amendments and remarks have clearly overcome the objection and rejection set forth in the Office Action dated March 11, 2004. Applicants' remarks have distinguished claims 32 and 37 from Taya and thus overcome the rejection of these claims under 35 U.S.C. §103(a) and the objection to claims 21-23. Accordingly, Applicants request reconsideration and allowance of claims 21-23, 32 and 37.

Applicants submit that the application is now in condition for allowance. If the Examiner believes that the application is not in condition for allowance, Applicants respectfully request that the Examiner contact the undersigned attorney by telephone if it is believed that such contact will expedite the prosecution of the application.

In the event this paper is not considered to be timely filed, Applicants respectfully petition for an appropriate extension of time. The Commissioner is authorized to charge payment for any additional fees, which may be required with respect to this paper or credit any overpayment to Counsel's Deposit Account 01-2300, referring to client-matter number 024016-00012.

Respectfully submitted,

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